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Feb. 14. 2006 9:56AM Walker & Sako, LLP

No. 1781 P. 1

FEB 1 4 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE Applicant(s): Uneme, Masakatsu Group Art Unit: 2186 Serial No.: 10/657,464 Filed: September 8, 2003 Examiner: Kim, Hong Chong (As Amended) Data Processing Title: Single **Apparatus** that Shares Among Semiconductor Memory Circuit Multiple Data Processing Circuits Attorney Docket No.: N26532602E TRANSMITTAL COVER SHEET (37 C.F.R. §1.8(a)(i)(A)) First Class Mail **Assistant Commissioner for Patents** Washington, D.C. 20231 The following is included: Applications Amendment/Response Response to Missing Parts Under 37 After Final Rejection ſl C.F.R. §1.52 or §1.53 Affidavits/Declaration(s) **[**] Assignment Papers Extension of Time Request ГЪ Power of Attorney/Revocation/Change Information Disclosure Statement [] of Correspondence Address Status Request Letter [] Other Certification Under 37 C.F.R. 1.8(b) [X]Conditional Petition for Extension of Time It is believed that the indicated items are timely filed. However, in the event an extension of time is required, please consider this a petition for extension of time under 37 C.F.R. §1.136(a). Please charge any fees that may be required to Deposit Account No. 50-2087. Respectfully Submitted, February 14, 2006 37 C.F.R. \$1.8 I hereby certify that this correspondence is being [X] transmitted via facsimile to the United States Patent and Trademark Office to fax number: 1-571-273-8300 Date of Transmittal: February 14, 2006 [] deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231. Date of Deposit: Typed/Printed Name: Darryl G. Walker Signature:

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No. 1781 P. 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Uneme, Masakatsu

Serial No.: 10/657,464

Filed: September 8, 2003

Title: (As Amended) Data Processing Apparatus that Shares a Single Semiconductor Memory Circuit Among

Multiple Data Processing Circuits

Attorney Docket No.: N26532602E

Group Art Unit: 2186

Examiner: Kim, Hong Chong

CERTIFICATION OF PREVIOUS TRANSMISSION/DEPOSIT 37 C.F.R. 1.8(b)

Statement of **Darryl G. Walker**:

- (1) Examiner H. C. Kim contacted me by telephone on February 10, 2006 to inform me that a faxed in response to an Office Action ("the Correspondence") dated December 16, 2005 for case serial no. 10/657,464 was incomplete, and needed to be re-submitted.
- (2) Transmitted herewith is a copy of the previously transmitted Correspondence which includes a certification under 37 C.F.R. 1.8(a) indicating that the Correspondence was transmitted to the Patent Office on <u>December 16, 2005</u>.
- (3) I transmitted the Correspondence to the fax number <u>1-571-273-8300</u> on December 16, 2005. Included are the following:
- a) a copy of the sending unit's report confirming the transmission of the Correspondence.
- b) a copy of a first Auto-Reply Facsimile Transmission confirming the receipt of the first six pages of the Correspondence.
- c) a copy of a second Auto-Reply Facsimile Transmission confirming the receipt of the last ten pages of the Correspondence.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Signed:	
Dulh	February 14, 2006
Darryl G. Walker Reg. No. 43,232	Date

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Feb. 14. 2006 9:57AM Walker & Sako, LLP

FEB 1 4 2006

No. 1781 P. 4

AMENDMENT TRANSMITTAL LETTER						Attorney Docket No: N26532602E
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Alexandria, VA 22313				envelope addressed	to: Commissione	or for Patents, Box 1450,
Typed/Printed Name:	Darryl G. V	Valker				

No. 1781 P. 20 P. 1

* * * Communication Result Report (Dec. 16. 2005 10:30AM) * * *

Date/Time: Dec. 16. 2005 10:21AM

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E. 3) No answer
E. 5) Exceeded max. E-mail size

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Dec. 6. 1985 10:23AV 3: kei § 34.0...P IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

11. (Original) The data processing apparatus of claim 9, wherein:

each of the plurality of data processing circuits includes

a request input/output (I/O) for indicating when the data processing

circuit seeks control of the semiconductor memory circuit,

a grunt I/O for indicating when the data processing choult is granted control of the semiconductor memory circuit, and

a busy I/O for indicating when the data processing circuit is controlling the semiconductor memory circuit.

12. (Original) The data processing apparatus of stain 11, wherein:

each of the plurality of data processing circuits includes

a first switch for solectively connecting the request I/O, grant I/O, and busy I/O to a requesting circuit that generates a request indication and busy indication for the data processing circuit, and

a second switch for selectively connecting the request I/O, grant VO, and busy VO to an arbitration circuit that generates a grant indication:

the first awitch is disabled and the second switch is emplied when the data processing circuit is initialized as a master device, and the first switch is enabled and the second switch is disabled when the data

processing circuit is initialized as a slave device.

13. (Original) The data processing apparatus of claim 12, wherein:

each data processing circuit includes

a controller that generates at least one controller signal for enabling or disabling the first switch and second switch according to initialization

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14. (Original) The data processing apparatus of claim 9, wherein:

the or least one control line is directly connected to the control input of the semiconductor memory circuit end the control output of each of the plurality of

data processing circuits.

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